REMARKS

The present Amendment cancels claims 1-22 and adds new claims 23-32. Therefore, the present application has pending claims 23-32.

New claims 23-32 were drafted so as to correspond to the elected invention particularly the invention of Group II, claims 7-11, 21 and 22.

In paragraph 8 of the Office Action the Examiner objected to the originally filed Declaration. Filed on November 1, 2004 was a Supplemental Declaration which was signed and dated by all the inventors including the ninth inventor, Mr. Satoshi TAIRA. Therefore, the Examiner's objection to the originally filed Declaration is overcome and should be withdrawn.

Figs. 1-4 stand objected to being that the Examiner alleges that these figures should be designated by a legend "Prior Art". Filed on even date herewith are Replacement Sheets adding the legend "Prior Art" to Figs. 1 and 2. It should be noted however, that Figs. 3 and 4 were used to describe features of the present invention and such description was set forth, for example, in the "Description of the Preferred Embodiment" section of present application beginning on page 59, line 21 through page 62, line 3 and in the "Summary of the Invention" section of the present application beginning on page 5, line 23, through page 6, line 5, respectively. Thus, adding a legend "Prior Art" to Figs. 3 and 4 would be an incorrect designation and as such would add confusion to the description of the present invention. Therefore, the legend "Prior Art" was not added to Figs. 3 and 4 as requested by the Examiner. However, labels missing from the elements illustrated in Fig. 3 were added.

Approval of the Replacement Sheets is respectfully requested.

The specification was reviewed to uncover any possible minor errors. However, no such errors were detected. The Examiner is respectfully requested to point to any errors the Examiner may aware of so that such errors can be corrected so as to expedite prosecution of the present application.

Claims 7, 8, 10, 11, 21 and 22 stand rejected under 35 USC §112, second paragraph as being indefinite for failing to particularly point out and distinctly claim the subject matter which Applicants regards as the invention. As indicated above, claims 7, 8, 10, 11, 21 and 22 were canceled. Therefore, this rejection with respect to these claims is rendered moot. Accordingly, reconsideration and withdrawal of this rejection is respectfully requested.

Claims 7-11 and 21 stand rejected under 35 USC §102(b) as being anticipated by Morris (U.S. Patent No. 4,503,287); and claim 22 stands rejected under 35 USC §103(a) as being unpatentable over Morris in view of Shelton (U.S. Patent No. 6,035,380). As indicated above, claims 7-11, 21 and 22 were canceled. Therefore, these rejections are rendered moot. Accordingly, reconsideration and withdrawal of these rejections is respectfully requested.

It should be noted that the cancellation of claims 7-11, 21 and 22 was not intended nor should it be considered as an agreement on Applicants part that the features recited in claims 7-11, 21 and 22 are taught or suggested by any of the references of record whether taken individually or in combination with each other. The cancellation of claims 7-11, 21 and 22 was simply intended to expedite prosecution of the present application in favor of claims that more clearly recite features of the present invention.

New claims 23-32 are directed to a semiconductor chip in which information of two values correspond to two different voltages. As recited in the claims, the semiconductor chip includes a information processing device 0601, an information memory device 0602, an encryption device 0603, a decryption device 0604 and a data bus 0605. These features of the present invention are illustrated, for example, in Fig. 14 of the present application.

According to the present invention, data is transferred from the information processing device 0601 to the information memory device 0602 through the data bus 0605 and stored in the information memory device 0602 after the data have been encrypted by the encryption device 0603 and the data read from the information memory device 0602 is input into the information processing device 0601 through the data bus 0605 after the data has been decrypted by the decryption device 0604.

Alternatively, the semiconductor chip could include, for example, an information processing device, an information memory device, a first encryption device, a second encryption device, a first decryption device, a second decryption device and a data bus. As recited in the alternative embodiment, data output from the information processing device is encrypted by the first encryption device and output through the data bus, data encrypted by the first encryption device is transferred to the first decryption device through the data bus, decrypted by the first decryption device and stored in the information memory device, data read from the information memory device is encryption device and output to the data bus and data encrypted by the second encryption device is transferred to the second decryption

device through the data bus, decrypted by the second decryption device and input to the information processing device.

The above described features of the present invention are not taught or suggested by any of the references of record whether taken individually or in combination with each other. Particularly, the above described features of the present invention are not taught or suggested by Morris or Shelton whether taken individually or in combination with each other as suggested by the Examiner.

Morris teaches, for example, in Fig. 2 thereof a two-tiered communications system which employs asymmetric session keys so as to implement communication security between a host computer and another remote computer or terminal. As illustrated in Fig. 2, Morris provides encryption/decryption apparatus for encrypting/decryption information between the host 12 of the telecommunication system and the client 16. However, at no point is there any teaching or suggestion in Morris of the above described features of the present invention as now more clearly recited in the claims. Particularly, Morris fails to teach or suggest that data is encrypted on a data bus in a semiconductor chip such that data between an information processing device and an information memory device is encrypted or decrypted as recited in the claims. There is no teaching or suggestion at any point in Morris regarding the encrypting or decrypting of data between an information processing device and information memory device on a data bus in semiconductor chip as in the present invention.

Thus, Morris fails to teach or suggest a semiconductor chip in which information of two values correspond to two different voltages, wherein the

semiconductor chip includes an information processing device, an information memory device, an encryption device, a decryption device and a data bus as recited in the claims.

Further, Morris fails to teach or suggest that data is transferred from the information processing device to the information memory device through the data bus and stored in the information memory device after the data haa been encrypted by the encryption device and that data read from the information memory device is input into the information processing device through the data bus after the data has been decrypted by the decryption device as recited in the claims.

Still further, Morris fails to teach or suggest a semiconductor chip in which information of two values corresponds to two different voltages wherein the semiconductor chip includes an information processing device, an information memory device, a first encryption device, a second encryption device, a first decryption device, a second decryption device and a data bus as recited in the claims.

Even further yet, Morris fails to teach or suggest that data output from the information processing device is encrypted by the first encryption device and output to the data bus, that the data encrypted by the first encryption device is transferred to the first decryption device through the data bus, decrypted by the first decryption device and stored in the memory device, that data read from the information memory device is encrypted by the second encryption device and output to the data bus and that data encrypted by the second encryption device is transferred to the second

decryption device through the data bus, decrypted by the second decryption device and input to the information processing device as recited in the claims.

Therefore, the features of the present invention as now more clearly recited in the claims are not taught or suggested by Morris whether taken individually or in combination with any of the other references of record.

The above described deficiencies of Morris are not supplied by any of the other references of record. Particularly, these deficiencies of Morris are not supplied Shelton.

Shelton teaches an integrated circuit. However, at no point is there any teaching or suggestion in Shelton of the above described features of the present invention regarding the semiconductor chip including an information processing device, an information memory device, an encryption device, a decryption device and a data bus as now more clearly recited in the claims. Particularly, there is no teaching or suggestion in Shelton that data transmitted between the information processing device and the information memory device is subject to either a decryption or encryption function as in the present invention.

Therefore, the features of the present invention are not taught or suggested by Morris whether taken individually or in combination with Shelton.

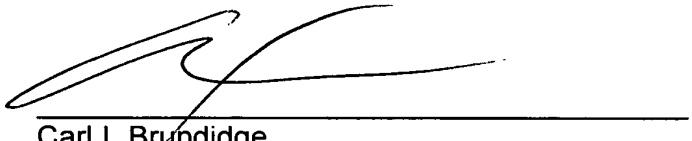
The remaining references of record have been studied. Applicants submit that they do not supply any of the deficiencies noted above with respect to the references utilized in the rejection of claims 7-11, 21 and 22.

In view of the foregoing amendments and remarks, applicants submit that claims 23-32 are in condition for allowance. Accordingly, early allowance of claims 23-32 is respectfully requested.

To the extent necessary, the applicants petition for an extension of time under 37 CFR 1.136. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, or credit any overpayment of fees, to the deposit account of MATTINGLY, STANGER & MALUR, P.C., Deposit Account No. 50-1417 (520.38691X00).

Respectfully submitted,

MATTINGLY, STANGER & MALUR, P.C.



Carl I. Brundidge
Registration No. 29,621

CIB/jdc
(703) 684-1120